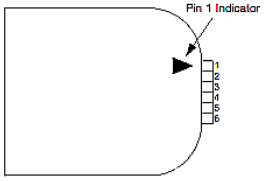
PICKit 2 Breadboard ICSP & Debug cable

A 25cm home built cable terminating in six colour coded individual 0.025" square pins for use with DIP PICs in solderless breadboards.

Pin functions

Pin	Colour		PIC ICSP	EEPROM	Logic Analyser	Logic Tool	UART tool
1	Yellow		Vpp or /MCLR		-nc-	Out 1	-nc-
2	Red		Vdd Target	Vdd Target	Vdd Target	Vdd Target	Vdd Target
3	Black		Vss (ground)	Vss (ground)	Vss (ground)	Vss (ground)	Vss (ground)
4	Blue		ICSPDAT or PGD		Chan 1	I/O 4	RX (in)
5	White		ICSPCLK or PGC		Chan 2	I/O 5	TX (out)
6	Green		AUX or PGM*(LVP only)*		Chan 3 (schmitt)	I/O 6 (schmitt)	-nc-



Notes: Vdd **must** either be connected or set to the same as (or slightly higher than) the Target board Vdd. Pins 4 & 5 have 4.7K pulldown resistors for the debugger which may affect their use as inputs. The UART tool is logic level ONLY. **Do NOT connect to RS232 levels**.

N.B. To avoid risk of damage to the PICkit 2, it **MUST** be disconnected from self powered targets while the PICkit 2 USB is disconnected or powered down.

DIP Chip Programming Connections (*CHECK THE DATASHEET*)

PICkit pin		1	2	3	4	5	6
Func.		Vpp & /MCLR	Vdd	Vss (ground)	ICSPDAT or PGD	ICSPCLK or PGC	PGM or Aux
Colour		Yellow	Red	Black	Blue	White	Green
Chip	**Pins**						
Generic PIC	8	4	1	8	7	6	-nc-
Generic PIC	14	4	1	14	13	12	-nc-
Generic PIC	18	4	14	5	13	12	9^{+}
Generic PIC	20	4	1	20	19	18	-nc-
Generic PIC	28	1	20	8,19	28	27	24^{+}
Generic PIC	40	1	11,32	12,31	40	39	36^{+}
PIC10F20x	8	8	2	7	5	4	-nc-
PIC18F2x5x ($)	28	1	20	8,19	28*	27*	26^{+}
24LC EEPROM	8	-nc-	8, A_x	4,7$_{wp}$, A_x	-nc-	6	5$^{\#}$
25LC EEPROM	8	1	8, 3$_{/wp}$, 7$_{/hold}$	4	2	6	5
93LC EEPROM	8	1	8, 7$_{pe}$,*C*	5, *C*	4	2	3

Generic PIC pinouts: *( ) indicates symbol in table*

This is a quick reference only. CHECK THE DATA SHEET. All ground and supply pins MUST be connected.

PGD and PGC filtering for newer PICS: *if direct connection fails*

($) Olin Lathrop on the Microchip forum, for the PIC18Fxxxx family, suggests adding 22 to 47 pF capacitors on the PGD and PGC lines to ground near the target chip with a 100 ohm resistor in the PGD line between the chip and the cap. This low pass filters the PGD signal when it is driven by the target chip, reducing the high frequencies that can couple onto the PGC line. The cap on the PGC line makes it less susceptible to coupled noise.

LVP Mode:

(+) The PGM pin is the most variable across families, but if all possible PGM pins for that package are grounded, HVP mode is guarantied. If LVP mode is wanted, connect the correct PGM pin to AUX and select 'Use LVP Program Entry' from the 'Tools' menu. It is possible to leave AUX disconnected and just ground the target pin to force HVP mode. Some families do not use HVP and have no PGM pin.

Other Notes:

(#) Pullup resistor required.

(*func*) Function of EEPROM pin tied to GROUND or Vdd.

(A_x, *C*) Tie address and word size select pins high or low as per datasheet.

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